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E-mail: infomep@madeeasy.in
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CHAPTER 2

Power Semi-conductor Diode and Transistor

2.1 Introduction

The increased power capabilities, ease of control and reduced cost of modern power semiconductor devices have made converters affordable in large number of applications and have opened up a host of new converter topologies for power electronic applications. In order to clearly understand the feasibility of these new topologies and applications, it is essential that the characteristics of available power devices be put in perspective.

Presently available power semiconductor devices can be classified into three groups according to their degree of controllability:

1. Diodes
2. Controllable switches (BJT, MOSFET, IGBT etc.)
3. Thyristor

The objective of this chapter is to describe power diode and power transistors.

2.2 Power Diode

2.2.1 Basic Structure and I-V Characteristics

Power diodes differ in structure from signal diodes. A signal diode constitutes a simple p-n junction. The intricacies in constructing power diodes arise from the need to make them suitable for high-voltage and high-current applications. Thus, a power diode should be so designed as to handle high forward current and a large reverse breakdown voltage.

The practical realization of diode for power application is shown below.

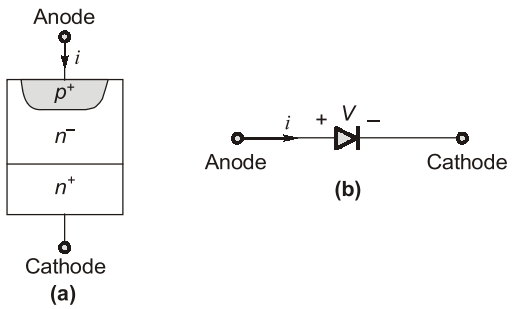


Fig. 2.1 : *(a) Circuit symbol of power diode (b) Structural feature of power diode*

It consists of a heavily doped *n*-type substrate on top which is grown a lightly doped 'n^-' epitaxial layer of specified thickness. Finally the *p*-*n* junction is formed by diffusing in a heavily doped p-type region that forms the anode of the diode.

The n^- layer which is often termed the drift region, is the prime structural feature not formed in low power diodes. Its function is to absorb the depletion layer of the reverse biased p^+ n^- junction.

This relatively long lightly doped region would appear to add significant ohmic resistance to the diode when it is forward biased.

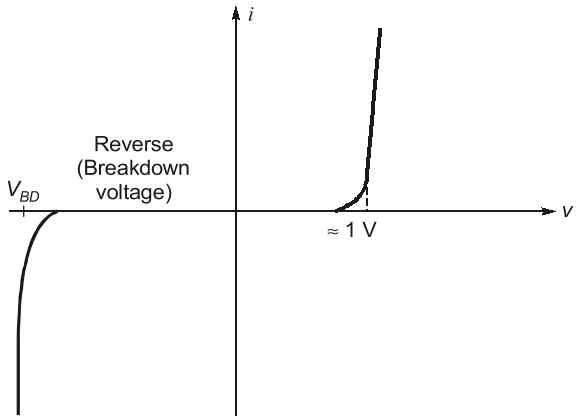


Fig. 2.2 : *(I-V characteristics of sources diode)*

The current grows linearly with the forward bias voltage rather than exponentially.

In reverse bias only a small leakage current, which is independent of the reverse voltage, flows until the reverse break down voltage V_{BD} is reached. When breakdown is reached the voltage appears to remain essentially constant while the current increases dramatically.

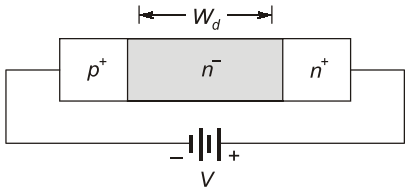


Fig. 2.3 : *(A forward bias power diode)*

If the length W_d of the lightly doped region is longer than the depletion layer width at breakdown, then the structure is termed a non punch through diode, that is, the depletion layer has not reached through (or punched through) the lightly doped drift region and reached the highly doped n^+ subtract.

Two basic facts; first, large breakdown voltages require lightly doped junctions, at least on one side. Second, the drift layer in the diode must be fairly long in high voltage devices to accommodate the long depletion layers.

2.2.2 Switching Characteristics

A power diode requires a finite time to switch from the blocking state (reverse bias) to the on state (forward bias) and vice versa.

The features of particular interest in these waveforms are the voltage overshoot during turn on and the sharpness of the fall of the reverse current during the turn off phase.

The overshoot of the voltage during turn on is not observed with signal level diodes.

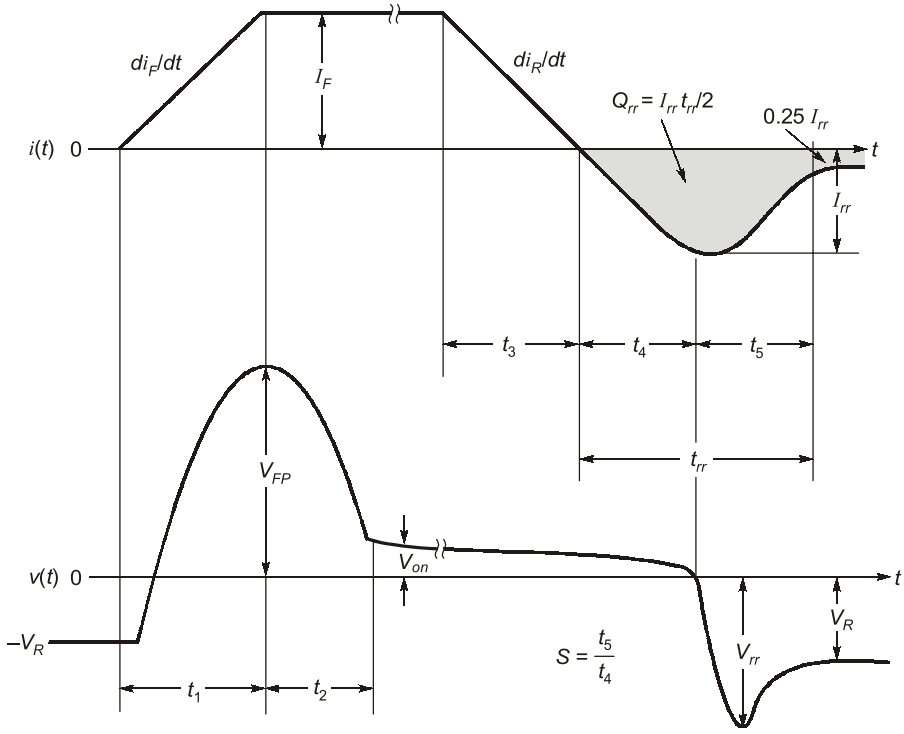


Fig. 2.4 : *Power diode switching characteristics*

1. Turn-on Transient

The turn on portion of the diode waveform is encompassed by the times labeled t_1 and t_2. During these intervals two physical process occur in sequence. First the space charge stored in the depletion region (located mainly in the drift region) because of the large reverse bias voltage is removed (discharged) by the growth of the forward current. When the depletion layer is discharged to its thermal equilibrium level, the metallurgical junction becomes forward biased and the injection of excess carriers across the junction into the drift region commences at time t_1, thus marking the start of the second phase and the end of the first. During the second phase, the excess-carrier distribution in the drift region grows towards the steadily state value that can be supported by the forward diode current I_f.

NOTE: Excess carries are injected into the drift region from both ends with holes being injected from the $p^+ n^-$ junction and electrons from the $n^+ n^-$ junction.

2. Turn-off Transient

The turn-off portion of the switching waveform is encompassed by the times labeled t_3, t_4 and t_5 and is essentially the inverse of the turn-on process. First the excess carriers stored in the drift region must be removed before the metallurgical junctions can become reverse biased.

Once the carriers are removed by the combined action of recombination and sweepout by negative diode currents, the depletion layer acquires a substantial amount of space charge from the reverse-bias voltage and expands into the drift region from both ends (junctions).

As long as there are excess carriers at the ends of the drift region, the $p^+ n^-$ and $n^+ n^-$ junctions must be forward biased. Thus, the diode voltage will be little changed from its on-state value except for a small decrease due to ohmic drops caused by the reverse current. But after the current goes negative and carrier sweepout has proceeded for a sufficient time (t_4) to reduce the excess-carrier density at one or both of the junctions to zero, the junction or junctions become reverse biased. At this point the diode voltage goes negative and rapidly acquires

substantial negative values as the depletion regions from the two junctions expand into the drift region toward each other. At this time the negative diode current demanded by the stray inductance of the external circuit cannot be supported by the excess-carrier distribution because too few carriers remain. The diode current ceases its growth in the negative direction and quickly falls, becoming zero after a time t_5. The reverse current has its maximum reverse value, I_{rr}, at the end of the t_4 interval.

2.2.3 Reverse Recovery Characteristics

The current in a forward-biased junction diode is due to the net effect of majority and minority carriers. Once a diode is in a forward conduction mode and then its forward current is reduced to zero (due to the natural behaviour of the diode circuit or application of a reverse voltage), the diode continues to conduct due to minority carriers that remain stored in the pn-junction and the bulk semiconductor material. The minority carriers require a certain time to recombine with opposite charges and to be neutralized. This time is called the reverse time of the diode.

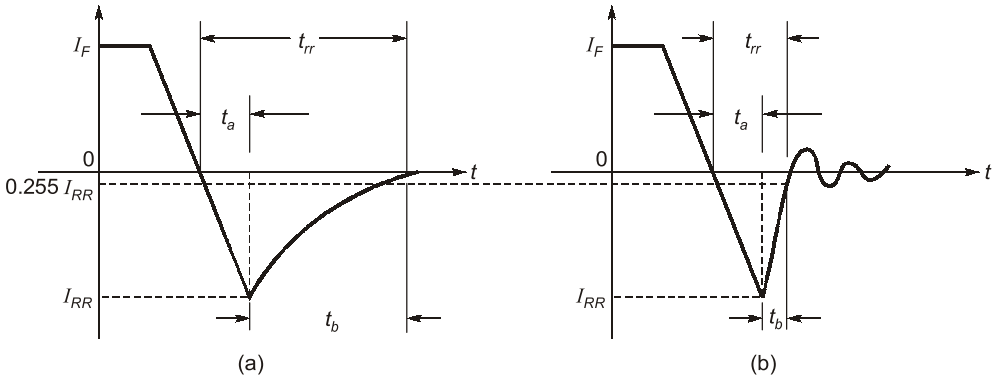


Fig. 2.5 : *Reverse recovery characteristics (a) Soft recovery (b) Abrupt recovery*

The time interval $t_{rr} = t_4 + t_5$ shown in the graph is often termed the reverse recovery time. Its characteristics are important in almost all power electronic circuits where diode are used.

t_{rr} = reverse recovery time

Q_{rr} = reverse recovery charge

$\frac{di_R}{dt}$ = rate of change of reverse current

S = snappishness factor or softness factor

There quantities are inter related to each other.

We note that I_{rr} can be written as,

$$I_{rr} = \frac{di_R}{dt} \times t_4$$

$\because$ $$\boxed{SF = \frac{t_5}{t_4}}$$

$$t_4 = t_{rr} - t_s = t_{rr} - SF\ t_4$$

$$t_4 = \frac{t_{rr}}{SF + 1}$$

$$t_4 = t_{rr} - t_5 = \frac{t_{rr}}{SF + 1}$$

$\therefore$ $$I_{rr} = \frac{di_R}{dt} \times \frac{t_{rr}}{SF + 1}$$

$$Q_{rr} \cong \frac{1}{2} I_{rr} t_{rr}$$

So that, $$Q_{rr} = \frac{di_R}{dt} \frac{t_{rr}^2}{2(SF+1)}$$

Reverse recovery time, $$t_{rr} = \sqrt{\frac{2Q_{rr}(1+SF)}{\left(\frac{di_R}{dt}\right)}}$$; $$I_{rr} = \sqrt{\frac{2Q_{rr}\left(\frac{di_R}{dt}\right)}{(SF+1)}}$$

The charge Q_{rr} represents the portion of the total charge Q_F (the charge stored in the diode during forward bias), which is sweepout by the reverse current and not lost to internal recombination. Most of Q_F is stored in the drift region.

2.2.4 Power Diode Types

Ideally, a diode should have no reverse recovery time. However, the manufacturing cost of such a diode may increase. In many applications, the effects of reverse recovery time is not significant, and inexpensive diode can be used. Depending on the recovery characteristics and manufacturing techniques, the power diodes can be classified into the following three categories:

1. Standard or general -purpose diodes
2. Fast-recovery diodes
3. Schottky diodes

The characteristics and practical limitations of these types restrict their applications.

1. General Purpose Diodes

The general purpose rectifier diodes have relatively high reverse recovery time, typically 25 μs; and are used in low-speed applications, where recovery time is not critical (e.g. diode rectifiers and converters for allow-input frequency up to 1 kHz applications and line commutated converters). These diodes cover ratings from less than 1 A to several thousands of amperes, with voltage ratings from 50 V to around 5 kV. These diodes are generally manufactured by diffusion. However, alloyed types of rectifiers that are used in welding power supplies are most cost-effective and rugged, and their ratings can go up to 1500 V, 400 A.

2. Fast Recovery Diodes

The fast-recovery diodes have low recovery time, normally less than 5 μs. They are used in dc-dc converter circuits, where the speed of recovery is often of critical importance. These diodes cover current ratings of voltage from 50 V to around 3 kV, and from less than 1 A to hundreds or amperes.

For voltage ratings above 400 V, fast-recovery diodes are generally made by diffusion and the recovery time is controlled by platinum or gold diffusion. For voltage ratings below 400 V, epitaxial diodes provide faster switching speeds than those of diffused diodes. The epitaxial diodes have a narrow base width, resulting in a fast recovery time of as low as 50 ns.

3. Schottky Diodes

The charge storage problem of a pn-junction can be eliminated (or minimized) in a Schottky diode. It is accomplished by setting up a "barrier potential" with a contact between a metal and a semiconductor. A layer of metal is deposited on a thin epitaxial layer of *n*-type silicon. The potential barrier simulates the behaviour of a pn-junction. The rectifying action depends on the majority carriers only, and as a result there are no excess minority carriers to recombine. The recovery effect is due solely to the self capacitance of the semiconductor junction.

The recovered charge of a Schottky diode is much less than half of an equivalent pn-junction diode. Because it is due to the junction capacitance, it is largely independent of the reverse *di*/*dt*. A Schottky diode has a relatively low forward voltage drop.

The leakage current of a Schottky diode is higher than that of a pn-junction diode. A Schottky diode with relatively low conduction voltage has relatively high leakage current, and vice-versa. As a result, the maximum allowable voltage of this diode is generally limited to 100 V. The current ratings of Schottky diodes vary from 1 to 400 A. The Schottky diodes are ideal for high current and low voltage dc power supplies. However, these diodes are also used in low current supplies for increased efficiency.

2.3 Power Bipolar Junction Transistor : (Power BJT)

A bipolar transistor is formed by adding a second p^- or n^- region to pn-junction diode. With two n^- regions and one p^- regions, two junctions are formed and it is known as an NPN-transistor, as shown in Fig 2.6 (a). With two p^- regions and one n^- regions, it is called as PNP-transistor, as shown in Fig. 2.6 (b). The three terminals are named as collector, emitter, and base. A bipolar transistor has two junctions, collector base junction (CBJ) and base emitter junction (BEJ).

There are two n^+ regions for the emitter of NPN-type transistor shown in Fig. 2.6 (a) and two p^+ regions for the emitter of the PNP type transistor shown in Fig. 2.6 (b). For an NPN type, the emitter side *n*-layer is made wide, the p-base is narrow, and the collector side n-layer is narrow and heavily doped. For a PNP-type, the emitter side p-layer is made wide, the n-base is narrow, and the collector side p-layer is narrow and heavily doped. The base and collector currents flow through two parallel paths, resulting in a low on-state collector-emitter resistance, $R_{CE(ON)}$.

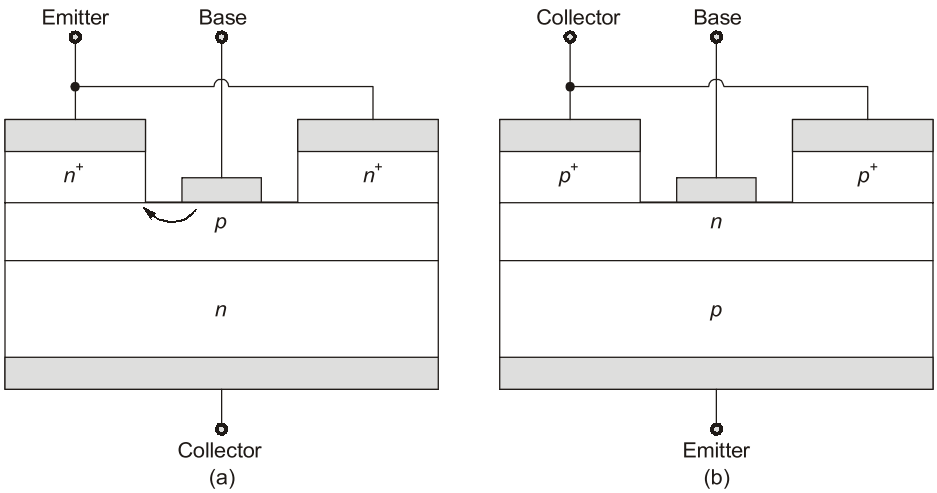


Fig. 2.6 : *(a) NPN-transistor (b) PNP-transistor*

NOTE: *npn* transistors are much more widely used than *pnp* transistor as power switches.

The doping levels in each of the layers and the thickness of the layers have a significant effect on the characteristics of the device. The doping in the emitter layer is quite large, where as the base doping is moderate. The n^- region that forms the collector half of the *C-B* (collector base) junction is usually termed the collector drift region and has a light doping level. The n^+ region that terminates the drift region has a doping level similar to that found in the emitter.

NOTE: The thickness of the drift region determines the breakdown voltage of the transistor.

2.3.1 I-V Characteristics of Power BJT

The output characteristics (I_C versus V_{CE}) of a typical *npn* power transistor are shown above. The various curves are distinguished from each other by the value of the base current. There is a maximum collector-emitter voltage that can be sustained across the transistor when it is carrying substantial collector current. In the limit of zero base current, the maximum voltage between collector and emitter that can be sustained increase some what to a value the collector emitter breakdown voltage when the base is open circuited. This voltage is measure of the transistor's voltage standoff capability because usually the only time the transistor will see large voltages is when the base current is zero and the BJT is in cut-off.

There are three operating regions of a transistor: cut-off, active, and saturation. In the cut-off region, the transistor is off or the base current is not enough to turn it on and both junctions are reverse biased. In the active region, the transistor acts as an amplifier, where the base current is amplified by a gain and the collector-emitter voltage decreases with the base current. The CBJ is reverse biased, and the BEJ is forward biased. In the saturation region, the base current is sufficiently high so that the collector-emitter voltage is low, and the transistor acts as a switch. Both junctions (CBJ and BEJ) are forward biased.

The voltage BV_{CBO} is the collector base breakdown voltage when the emitter is open circuited.

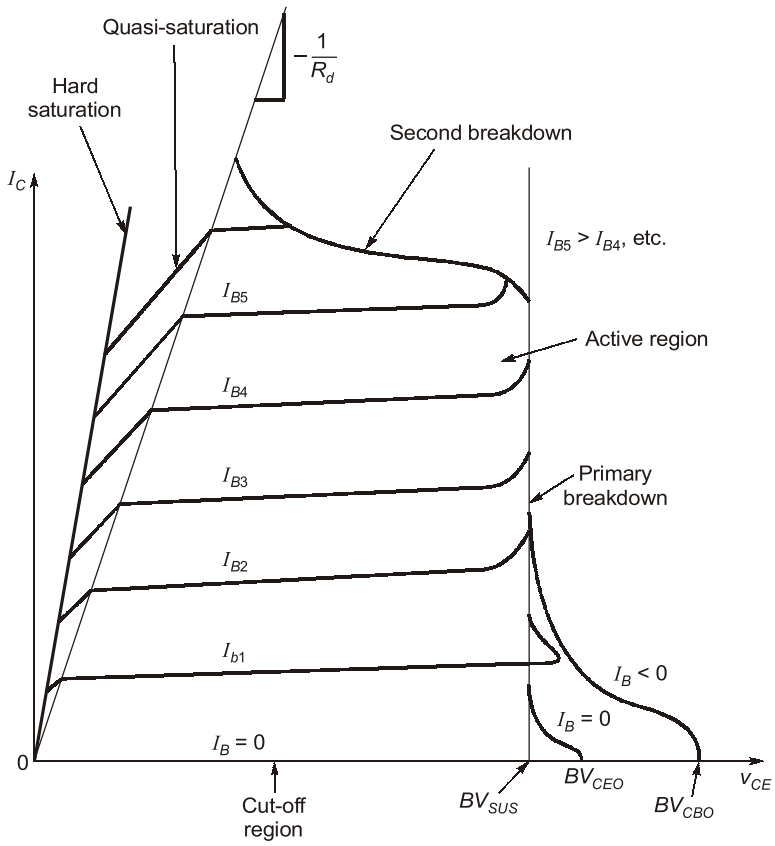


Fig. 2.7 : *i-v characteristics of power BJT*

The region labeled primary breakdown is due to conventional avalanche breakdown of the CB junction and attendant large flow of current. This region of characteristics is to be avoided because of the large power dissipation that clearly accompanies such breakdown.

The major abusable difference between the *i-v* characteristics of a power transistor and those of a logic level transistor is the region labeled Quasi-Saturation on the power transistor characteristics.

2.3.2 Basic Power BJT Equations

The base current is effectively the input current and the collector current is the output current. The ratio of the collector current I_C, to base current I_B, is known as the forward current gain β_F:

$$\beta_F = h_{FE} = \frac{I_C}{I_B}$$

The collector current has two components: one due to the base current and the other is the leakage current of the CBJ.

$$I_C = \beta_F I_B + I_{CE}$$

where I_{CEO} is the collector-to-emitter leakage current with base open circuit and can be considered negligible compared to $\beta_F I_B$.

From equations,

$$I_E = I_B(1 + \beta_F) + I_{CEO}$$
$$\approx I_B(1 + \beta_F)$$

$$I_E \approx I_C\left(1+\frac{1}{\beta_F}\right) = I_C\frac{\beta_F + 1}{\beta_F}$$

Because $\beta_F >> 1$, the collector current can be expressed as,

$$I_C \approx \alpha_F I_E$$

where the constant α_F is related to β by

$$\alpha_F = \frac{\beta_F}{\beta F + 1}$$

or,

$$\beta_F = \frac{\alpha_F}{1-\alpha_F}$$

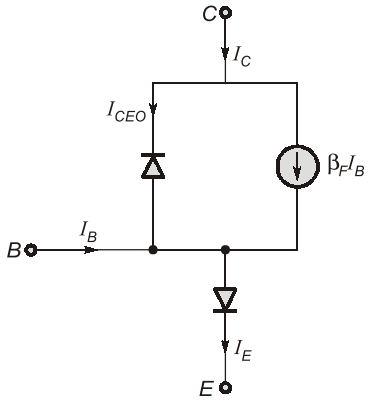


Fig. 2.8 : *Model of NPN-transistors*

2.3.3 BJT Switching Performance

When input voltage V_B to base circuit is made $-V_2$ at t_0, junction EB is reverse biased, $V_{BE} = -V_2$, the transistor is off, $i_B = i_C = 0$ and $V_{CE} = V_{CC}$.

At time t_1, base emitter voltage V_{BE} begins to rise gradually from $-V_2$ and collector current i_C begins to rise from zero and collector-emitter voltage V_{CE} starts falling from initial value V_{CC}. After some time delay t_d called delay time, the collector current rises to 0.1 I_{CS}, V_{CE} falls from V_{CC} to 0.9 V_{CC} and V_{BE} reaches V_{BES} = 0.7 V.

This delay time is required to charge the base emitter capacitance to V_{BES} = 0.7 V.

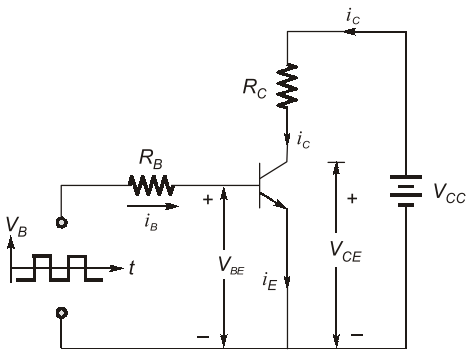


Fig. 2.9 : *Biased power BJT circuit*

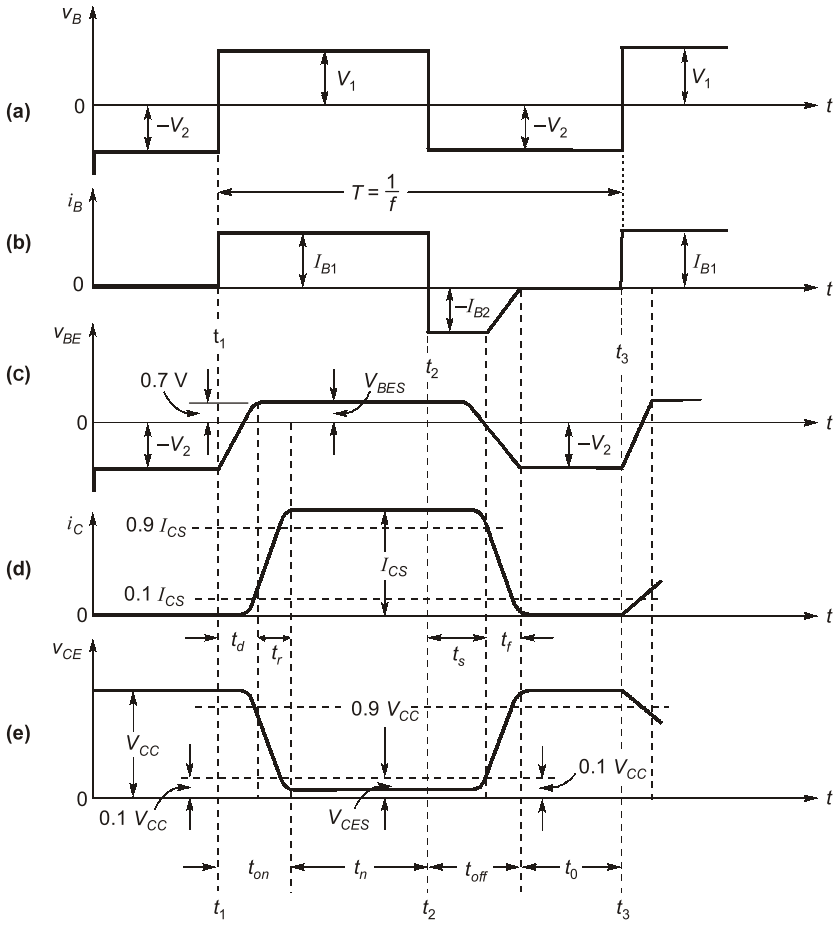


Fig. 2.10 : *Switching characteristics of power BJT*

Approximated Switching Characteristics

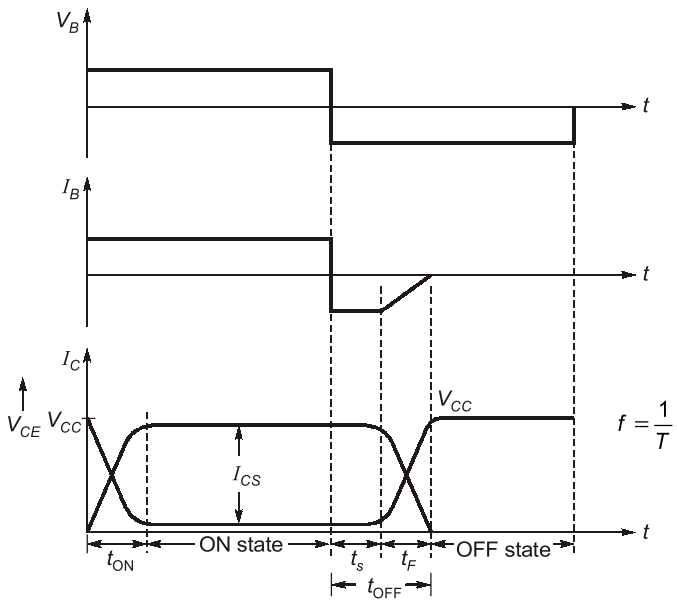


Fig. 2.11 : *Approximated switching characteristics*

NOTE

- Thus, delay time (t_d) is defined as the time during which the collector current rises from zero to 0.1 I_{CS} and collector emitter voltage falls from V_{CC} to 0.9 V_{CC}. After delay time t_d, collector current rises from 0.1 I_{CS} to 0.9 I_{CS} and V_{CE} falls from 0.9 V_{CC} to 0.1 V_{CC} in time t_r.
- This time t_r is known as rise time which depends up on transistor junction capacitance. Rise time (t_r) is defined as the time during which collector current rises from 0.1 I_{CS} to 0.9 I_{CS} and collector emitter voltage falls from 0.9 V_{CC} to 0.1 V_{CC}.
- The total turn on time is, $\boxed{t_{on} = t_d + t_r}$
- The time (t_s) required to remove these excess carriers is called storage time and only after t_s, base current I_{B2} begins to decrease towards zero.
  Transistor comes out of saturation only after t_s.
- Storage time (t_s) is defined as the time during which collector current falls from I_{CS} to 0.9 I_{CS} and collector emitter voltage V_{CE} rises from V_{CES} to 0.1 V_{CC}. After t_s, collector current begins to fall and collector emitter voltage starts building up. Time (t_f) called fall time, is defined as the time during which collector current drops from 0.9 I_{CS} to 0.1 I_{CS} and collector emitter voltage rise from 0.1 V_{CC} to 0.9 V_{CC}.

  Transistor turn off time, $\boxed{t_{off} = t_s + t_f}$

  t_n = conduction period of transistor
  t_o = off period
  f = switching frequency

  $T = \frac{1}{f}$ is the period time

2.3.4 Switching Limits

1. Second Breakdown (SB)

The SB, which is a destructive phenomenon, results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient, the excessive localized heating may damage the transistor. Thus, secondary breakdown is caused by a localized thermal runaway, resulting from high current concentrations. The current concentration may be caused by defects in the transistor structure. The SB occurs at certain combinations of voltage, current, and time. Because the time is involved, the secondary breakdown is basically an energy dependent phenomenon.

2. Forward-Biased Safe Operating Area (FBSOA)

During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power handling capability of a transistor. The manufacturers usually provide the FBSOA indicates the $I_C - V_{CE}$ limits of the transistor; and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.

3. Reverse-Biased Safe Operating Area (RBSOA)

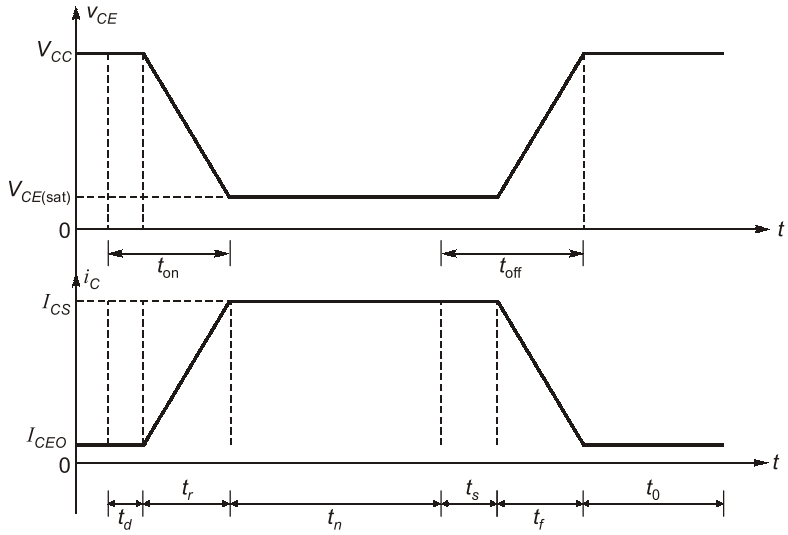
During turn-off, a high current and high voltage must be sustained by the transistor, in most cases with the base-to-emitter junction reverse biased. The collector emitter voltage must be held to a safe level at, or below, a specified value of collector current. The manufacturers provide the $I_C - V_{CE}$ limits during reverse-biased turn-off as RBSOA.

4. Breakdown Voltages

A breakdown voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted, or biased in either forward or reverse direction. At breakdown the voltage remains relatively constant, where the current rises rapidly. The following breakdown voltages are quoted by the manufacturers:

- V_{EBO}: The maximum voltage between the emitter terminal and base terminal with collector terminal open circuited.
- V_{CEV} or V_{CEX}: The maximum voltage between the collector terminal and emitter terminal at a specified negative voltage applied between base and emitter.
- $V_{CEO(SUS)}$: The maximum sustaining voltage between the collector terminal and emitter terminal with the base open circuited. This rating is specified at the maximum collector current and voltage, appearing simultaneously across the device with a specified value of load inductance.

Example-2.1 The waveforms of a transistor switch are shown below:



The parameters are V_{CC} = 250 V, $V_{CE\,(sat)}$ = 2 V, I_{CS} = 100 A, t_d = 0.5 µs, t_r = 1 µs, duty cycle = 50%, f_s = 10 kHz, I_{CEO} = 3 µA, t_s = 5 µs and t_f = 3 µs.

Determine the power loss due to collector current:

(i) During turn on period, $t_{on} = t_d + t_r$

(ii) During conduction period, t_n

(iii) During turn off period, $t_{off} = t_s + t_f$

(iv) During off-time, t_0

Solution:

$$T = \frac{1}{f_s} = 100\ \mu s$$

$$k = 0.5$$

$$kT = 0.5\,(100 \times 10^{-6}) = 50\ \mu s$$

$$t_d + t_r + t_n = 50\ \mu s$$

$$t_n = 50 - 0.5 - 1 = 48.5\ \mu s$$

$$(1 - k)T = t_s + t_f + t_0 = 50\ \mu s$$

and

$$t_0 = 50 - 5 - 3 = 42\ \mu s$$

(i) During delay time, $0 \le t \le t_d$:

$$i_c(t) = I_{CEO}$$
$$v_{CE}(t) = V_{CC}$$

Instantaneous power due to collector current is

$$P_c(t) = i_c v_{CE} = I_{CEO} V_{CC}$$
$$= (3 \times 10^{-3})\,(250) = 0.75\ \Omega \quad \text{... (i)}$$

The average power loss during delay time is

$$P_d = \frac{1}{T}\int_0^{t_d} P_c(t)\,dt = I_{CEO} V_{CC} t_d f_s$$
$$= (3 \times 10^{-3})\,(250)\,(0.5 \times 10^{-6})\,(10 \times 10^3) = 3.75\ \text{mW}$$

During rise time, $0 \le t \le t_r$:

$$i_c(t) = \frac{I_{cs}}{t_r} \times t$$

$$v_{CE}(t) = V_{CC} + (V_{CE\,(\text{sat})} - V_{CC})\,\frac{t}{t_r}$$

$$P_c(t) = i_c v_{CE}(t) = \frac{I_{cs}}{t_r} \times t\left[V_{CC} + (V_{CE}(sat) - V_{CC})\frac{t}{t_r}\right]$$

$$P_r = \frac{1}{T}\int_0^{t_r} P_c(t)\,dt = f_s I_{cs} t_r\left[\frac{V_{CC}}{2} + \frac{V_{CE(sat)} - V_{CC}}{3}\right] = 42.33\ \text{W} \quad \text{...(ii)}$$

Total power loss during turn-on is,

$$P_{on} = P_d + P_r = 0.00375 + 42.33$$
$$= 42.33\ \text{W}$$

(ii) Conduction period, $0 \le t \le t_n$

$$i_c(t) = I_{cs}$$
$$v_{CE}(t) = V_{CE}(\text{sat})$$
$$P_c(t) = i_c V_{CE} = V_{CE(\text{sat})}\, I_{cs}$$
$$= 2 \times 100 = 200\ \text{W}$$

$$P_n = \frac{1}{T}\int_0^{t_n} P_c(t)\,dt = V_{CE(\text{sat})}\ I_{CS} t_n f_s$$
$$= (2)(100) \times (48.5 \times 10^{-6}) \times (10 \times 10^3) = 97\ \text{W}$$

(iii) Storage period, $0 \le t \le t_s$

$$i_c(t) = I_{CS}$$
$$v_{CE}(t) = V_{CE(\text{sat})}$$
$$P_c(t) = i_c v_{CE} = V_{CE\,(\text{sat})}\, I_{cs}$$

$$P_s = \frac{1}{T}\int_0^{t_s} V_{CE} I_{cs}\,dt = V_{CE(\text{sat})}\ I_{CS} t_s f_s$$
$$= 2 \times 100 \times (5 \times 10^{-6})\,(10 \times 10^3) = 10\ \Omega$$

Fall time, $0 \le t \le t_f$

$$i_c(t) = I_{CS}\left(1 - \frac{t}{t_f}\right), \text{ neglecting } I_{CEO}$$

$$v_{CE}(t) = \frac{V_{CC}}{t_f} \times t \text{ , neglecting } I_{CEO}$$

$$P_c(t) = i_c v_{CE} = V_{cc} I_{cs} \left[\left(1 - \frac{t}{t_f} \right) \frac{t}{t_f} \right]$$

$$P_f = \frac{1}{T} \int_0^{t_f} P_c(t)\, dt = \frac{V_{CC} I_{cs}}{6} \times t_f \times f_r$$

$$= \frac{250 \times 100 \times (3 \times 10^{-6})(10 \times 10^3)}{6} = 125\,\text{W}$$

Power loss during turn off is

$$P_{off} = P_s + P_f = 10 + 125 = 135 \text{ W}$$

(iv) Off period, $0 \le t \le t_0$

$$i_c(t) = I_{CEO}$$
$$V_{CE}(t) = V_{CC}$$
$$P_c(t) = i_c v_{CE} = I_{CEO}\, V_{CC}$$
$$= (3 \times 10^{-3})\,(250) = 0.75 \text{ W}$$

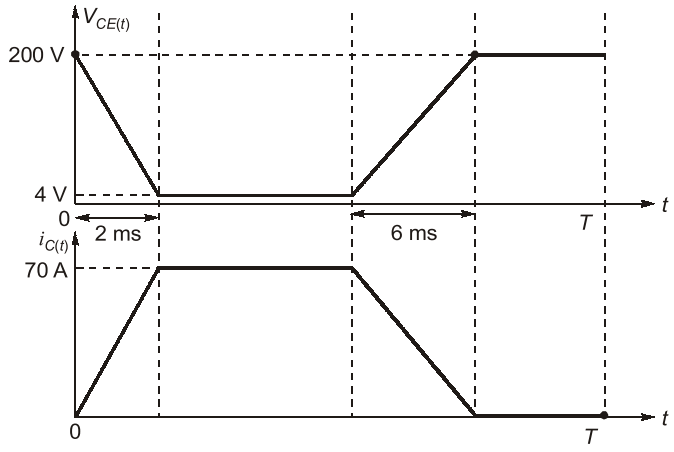
$$P_0 = \frac{1}{T} \int_0^{t_0} P_c(t)\, dt = I_{CEO} V_{CC} t_0 f_s$$

$$= (3 \times 10^{-3})\,(25°)\,(42 \times 10^{-6})\,(10 \times 10^3) = 0.315 \text{ W}$$

Example - 2.2 The switching waveforms of the transistor switch is shown in figure. Duty cycle α is 50% and switching frequency is 10 kHz.

Determine the average power loss due to collector current

(i) during turn on process.
(ii) during conduction period.
(iii) during turn off process.
(iv) during off state.
(v) Peak power loss during turn on process.
(vi) Total power loss in one cycle.



Solution:

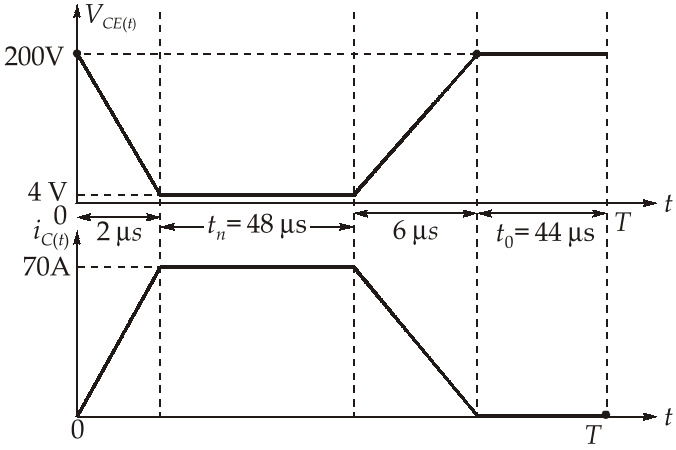
Duty ratio is given as $\alpha = 0.5$

$T_{on} = 0.05\ \mu s = 50\ \mu s$

conduction period $= 50 - 2 = 48\ \mu s$

off period $= 50 - 6 = 44\ \mu s$

Redrawing the waveforms, we get



Average power loss is given by,

$$P_C = \frac{1}{T}\int_0^t V_{CE}(t)\, i_C(t)\, dt \qquad \text{...(i)}$$

(i) During turn on process, $V_{CE(t)} = \left(\left(\frac{4-200}{t_{on}}\right)t + 200\right)$ V

and $i_{C(t)} = \left(\frac{70}{t_{on}}\right)t$ A

From equation (i), we get

Average power loss, $P_C = \frac{1}{T}\int_0^{t_{on}} \left(-\frac{196}{t_{on}}t + 200\right)\cdot\left(\frac{70}{t_{on}}\cdot t\right)dt$

$$= \frac{1}{T}\int_0^{t_{on}} \left(-\frac{196}{t_{on}^{\,2}}\cdot t^2 + \frac{200\times 70}{t_{on}}\cdot t\right)dt$$

$$= \frac{1}{T}\left[-\frac{196\times 70}{t_{on}^{\,2}}\cdot\frac{t^3}{3} + \frac{200\times 70}{t_{on}}\cdot\frac{t^2}{2}\right]_0^{t_{on}}$$

$$= f\left[-\frac{196\times 70\times t_{on}}{3} + \frac{200\times 70\times t_{on}}{2}\right]$$

$$= 10\times 10^3 \times\left[-\frac{196\times 70\times 2\times 10^{-6}}{3} + \frac{200\times 70\times 2\times 10^{-6}}{2}\right]$$

$$P_C = 48.533 \text{ W}$$

(ii) During conduction period,

$V_{CE}(t) = 4$ V

$i_C(t) = 70$ A

Average power loss, $P_C = \frac{1}{T}\int_0^{t_n} (4\times 70)\, dt$

$= 10 \times 10^3 \times 4 \times 70 \times 48 \times 10^{-6} = 134.4$ W

(iii) During turn off process,

$$V_{ce}(t) = \left(\frac{200-4}{t_{off}}\right)\cdot t + 4$$

$$i_c(t) = -\frac{70}{t_{off}}t + 70$$

Power loss,

$$P_c(t) = \frac{1}{T}\int_0^{t_{off}}\left(\left(\frac{196}{t_{off}}\right)\cdot t + 4\right)\cdot\left(-\frac{70}{t_{off}}t + 70\right)dt$$

$$= \frac{1}{T}\int_0^{t_{off}}\left[-\frac{196\times 70}{t_{off}^2}\cdot t^2 + \frac{196\times 70\times t}{t_{off}} + 4\times 70 + \left(\frac{-4\times 70t}{t_{off}}\right)\right]dt$$

$$= \frac{1}{T}\left[\frac{-196\times 70\times t^3}{t_{off}^2.3} + \frac{196\times 70\times t^2}{2t_{off}} + 4\times 70t - \frac{4\times 70}{2t_{off}}t^2\right]_0^{t_0}$$

$$= \frac{1}{T}\times t_{off}\left[-\frac{196\times 70}{3} + \frac{196\times 70}{2} + 4\times 70 - \frac{4\times 70}{2}\right] = 145.6\text{ W}$$

(iv) During off period,

$$V_{CE}(t) = 200\text{ V}$$
$$i_c(t) = 0$$
$$P_C = 0$$

(v) Peak power loss during turn on process,

$$P_C(t) = V_{CE}(t)\times i_C(t)$$

$$= \left[\left(-\frac{196}{t_{on}}\right)\cdot t + 200\right].\left[\frac{70}{t_{on}}\cdot t\right]$$

$$P_C(t) = \frac{-196\times 70}{t_{on}^2}\cdot t^2 + \frac{200\times 70}{t_{on}}.t$$

Power loss will be maximum at $t = t_m$ where $\frac{dP_C}{dt} = 0$

Therefore,

$$\frac{dP_C(t)}{dt} = \frac{-196\times 70}{t_{on}^2}\cdot 2t + \frac{200\times 70}{t_{on}}$$

$$0 = -\frac{196\times 70}{t_{on}^2}\cdot 2t_m + \frac{200\times 70}{t_{on}}$$

$$t_m = \frac{200\times 70\times t_{on}}{196\times 70\times 2} = 1.0204\ \mu\text{s}$$

Peak power loss will be

$$P_C(t) = -\frac{196\times 70}{t_{on}^2}\cdot t_m^2 + \frac{200\times 70}{t_{on}}\cdot t_m$$

$$P_C(t) = -3571.37 + 7142.8$$
$$P_C(t) = 3571.43\text{ W}$$

(vi) Total power loss in one cycle will be

$$P_T = 48.533 + 134.4 + 145.6 + 0$$
$$P_T = 328.533\text{ W}$$

2.4 Power MOSFET

Figure shows the structure of a typical n-channel power MOSFET. Note that the drain contact is on the bottom of the die, rather than on the top as it is in a signal-processing MOSFET. This structure gives maximum area to both drain and source contacts in order to produce a low-resistance connection to the package terminals. The polysilicon electrode gate is insulated from the source metal that covers it by a layer of SiO_2. The polysilicon gate electrode is connected by metal fingers that make contact through windows etched in the SiO_2.

Between the source and the drain regions are *p*-type material. These wells are known as the body region of the device. The channel of the MOSFET is formed on the surface of these *p*-wells just beneath the gate oxide.

The lightly doped *n*-type drain region is unique to power MOSFET, and is provided to allow growth of a long SCL, permitting the device to block a high voltage when it is off. In this respect, the region functions like the 'ν' region in a power BJT. This lightly doped drain region is frequently referred to as the extended drain or drift region. As the SCL grows, it pinches-off (depletes) the region between the *p*-wells, as shown in figure (the gate electrode acts as a field plate to promote this pinch-off). This feature of a power MOSFET's structure is important because it keeps the gate oxide from being subjected to the full drain voltage.

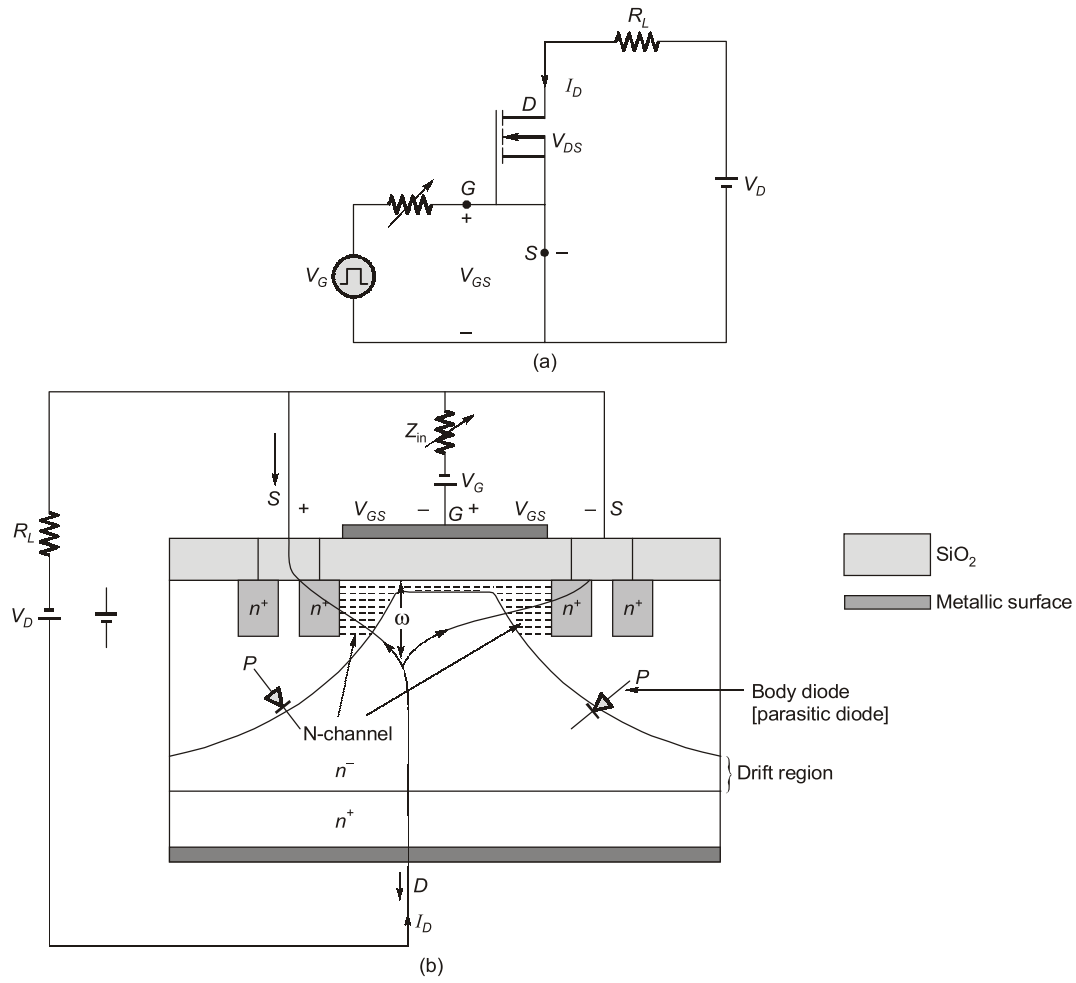


Fig. 2.12 : *(a) Basic power MOSFET circuit (b) Power MOSFET construction*

When gate signal is not given, V_D reverse biase the MOSFET. No path for I_D. So MOSFET is in cut-off region leakage current flows. When gate signal is given, +ve charges are induced near to metallic surface and other side –ve charge is induced. Acts as a capacitor. This n-channel provides path for drain around. Conduction is only due to $e^{-1}s$ (majority carriers. It is a majority carrier device. So it is a very high speed device.

When +ve gate signal is given, the n-channel is induced in *p* layer. This provides path for drain current. In MOSFET, conduction is only due to majority carriers (e^{-1} *s*). If is a majority carrier device. Due to the absence of minority charge carriers, the reverse recovery time is reduced very much. Therefore it operate with very high switching frequency.

2.4.1 Output Characteristics of Power MOSFET

As V_{GS} is ↑, I_D↑. For on state ohmic region is used. In active region, *V* drop is high. During ON state, MOSFET behaves as resistance (between drain and source). Between gate and source, it acts as capacitance *V* drop is not saturated here. It depends on I_D. In BJT, V drop is saturated. Does not depend on I_C. Conduction losses are more on MOSFET. Switching losses are more in BJT.

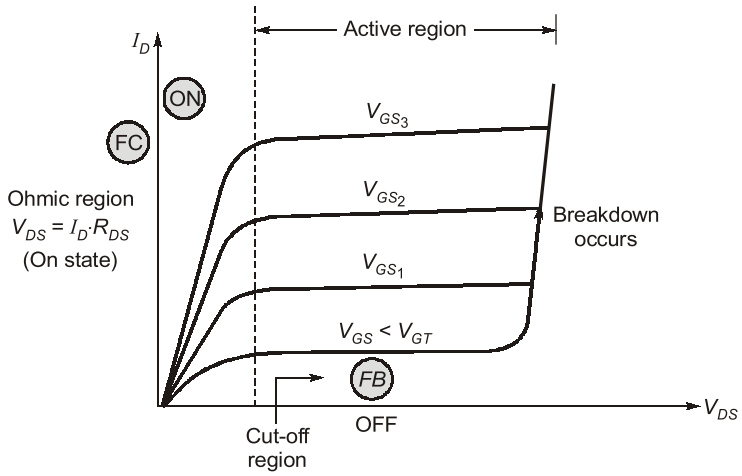


Fig. 2.13 : *Output characteristics of power MOSFET*

2.4.2 Body Diode Concept

When polarity of V_D is reversed, current flows from source to drain. There are inbuilt diodes called as body diode which allow reverse conduction MOSFET gives forward conduction.

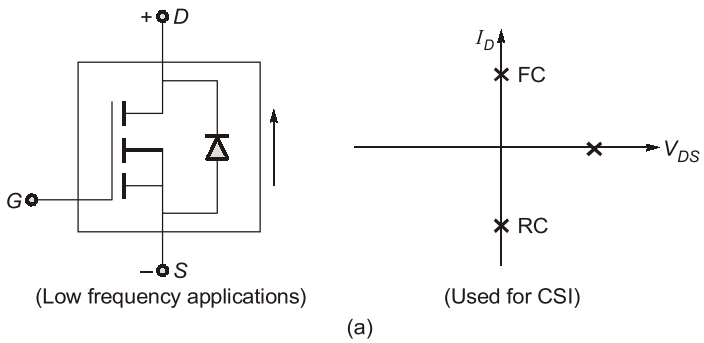


Fig. 2.14 (a)

MOSFET is high speed but body diode is slow minority carriers flow during conduction. So its speed as slow. To block the body diode, another series diode is used. This must be of high speed of utilize the complete switching frequency of MOSFET (Ex.: Schottky diode).

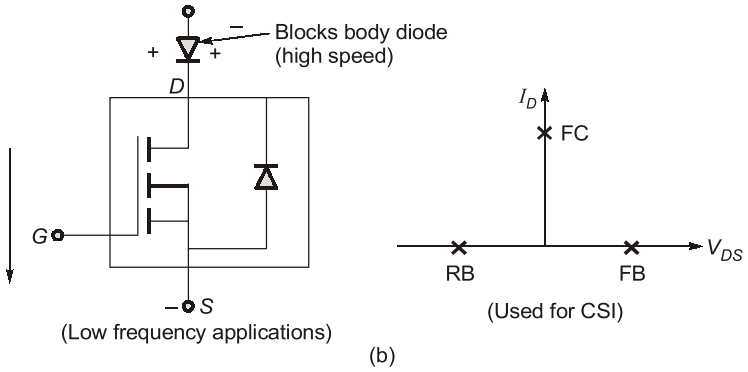


Fig. 2.14 (b)

2.4.3 Switching Characteristics of Power MOSFET

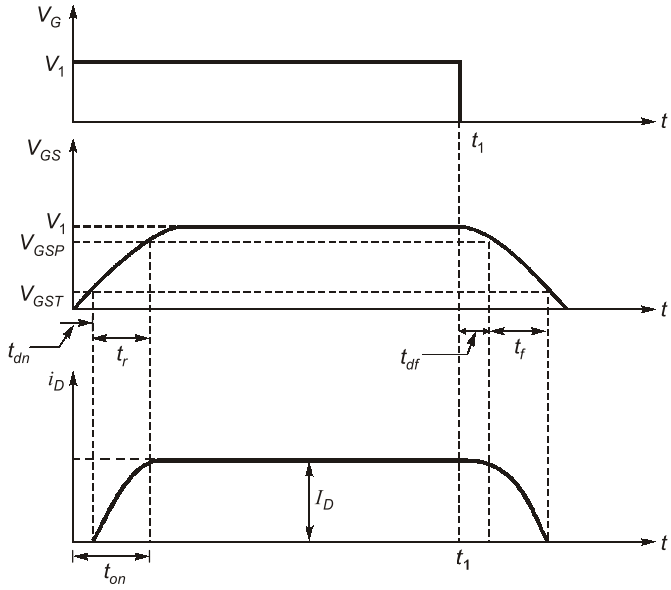


Fig. 2.15 : *Switching characteristics of power MOSFET*

- The switching characteristics of a power MOSFET are influenced to a large extent by the internal capacitance of the device and the internal impedance of the gate drive circuit. At turn-on, there is an initial delay t_{dn} during which input capacitance charges to gate threshold voltage V_{GST}. Here t_{dn} is called turn-on delay time.
- There is further delay t_r, called rise time, during which gate voltage rises to V_{GSP}, a voltage sufficient to drive the MOSFET into on state. During t_r, drain current rises from zero to full-on current I_D. Thus, the total turn on time is $t_{on} = t_{dn} + t_r$. The turn-on time can be reduced by using low-impedance gate-drive source.
- As MOSFET is a majority carrier device, turn-off proves is initiated soon after removal of gate voltage at time t_1. Time turn-off delay time, t_{df}, is the time during which input capacitance discharges from overdrive gate voltage V_1 to V_{GSP}. The fall time, t_f, is the time during which, input capacitance discharges from V_{GSP} to threshold voltage. During t_f, drain current falls from I_D to zero. So when $V_{GS} \leq V_{GST}$, PMOSFET turn-off is complete.